FORM PTO - 1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-060 APPLICANT(S): Lochtefeld *et al.* SERIAL NO.: 10/691,007 FILING DATE: October 22, 2003 GROUP: 2812

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EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A1	5,227,664	07/13/1993	Ueno			
	A2	6,268,253 B1	07/31/2001	Yu			
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	B1	0 784 339 A2	07/16/1997	EP				No	Yes
	B2	01/93338 A1	12/06/2001	WO				No	Yes

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EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C1 Imai *et al.* (May, 2002) "A 100 nm Node CMOS Technology for System-on-a-Chip Applications", IEICE Trans. Electron., Vol. E85-C, No. 5, pp. 1057-1063.
	C2 Park *et al.* (2002) "Gate Postdoping to Decouple Implant/Anneal for Gate, Source/Drain, and Extension: Maximizing Polysilicon Gate Activation for 0.1 μm CMOS Technologies", 2002 Symposium on VLSI Technology Digest of Technical Papers, pp. 134-135.
	C3 Reinking *et al.* (March, 1999) "Fabrication of high-mobility Ge p-channel MOSFETs on Si substrates", Electronics Letters, Vol. 35, No. 6, pp. 503-504.
	C4 Rim *et al.* (2002) "Characteristics and Device design of Sub-100 nm Strained SI N-and PMOSFETs", 2002 Symposium on VLSI Technology Digest of Technical Papers, pp. 98-99.
	C5 Su *et al.* (2000) "Strained $Si_{1-x}Ge_x$ graded channel PMOSFET grown by UHVCVD", Thin Solid Films, Elsevier Science, Vol. 369, No. 1-2, pp. 371-374.

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	C8	Xiang *et al.* (2000) "Very High Performance 40nm CMOS with Ultra-thin Nitride/Oxynitride Stack Gate Dielectric and Pre-doped Dual Poly-Si Gate Electrodes", International Electron Devices Meeting 2000 IEDM Technical Digest, pp. 860-862.
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